WHAT IS CLAIMED IS:

1. A turbo decoder comprising:

a first and a second error correction decoder for error-correction decoding encoded data;

an interleaver memory for storing a soft output decoded result calculated by said first decoder as an interleaver input sequence; and

an interleave address generator for generating write addresses for storing said interleaver input sequence in said interleaver memory, and read addresses for randomly reading an interleaver input sequence stored in said interleaver memory,

wherein said interleave address generator adds an offset to a symbol number for said interleaver input sequence for correction, and converts the corrected symbol number for said interleaver input sequence to generate the read address when an address for randomly reading the interleaver input sequence stored in said interleaver memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the interleaver input sequence.

2. A turbo decoder according to claim 1, wherein:

said interleave address generator specifies the symbol numbers for the interleaver input sequence as addresses at which the interleaver input sequence is stored in said interleaver memory, and

sequentially converts the symbol numbers for the interleaver input sequence stored in said interleaver memory to generate the read addresses for the interleaver input sequence stored in said interleaver memory.

3. A turbo decoder according to claim 2, wherein said interleave address generator comprises:

an output symbol number generator for sequentially generating symbol numbers for an interleaver input sequence stored in said interleaver memory; and

a threshold selector for setting a unique threshold for each of the symbol numbers generated by said output symbol number generator.

4. A turbo decoder according to claim 3, wherein:

said threshold selector selects a plurality of thresholds in accordance with the number of information bits of said interleaver input sequence, wherein said thresholds each correspond to an output symbol number generated by said output symbol number generator for each of the number of information bits of said interleaver input sequence, said output symbol number generator possibly generating an address, the value of which exceeds the number of bits excluding tail bits from the number of information bits of said interleaver input sequence.

5. A turbo decoder according to claim 4,

wherein:

said interleave address generator comprises an offset selector for selecting an offset, said offset being added to the output symbol number from said output symbol number generator, in accordance with a threshold value selected from said threshold selector.

6. A radio base station having an antenna, a radio frequency unit, a baseband unit, and a communication interface for interfacing said baseband unit with a communication network, wherein:

said baseband unit comprises a turbo decoder for decoding encoded data, said turbo decoder including:

a first and a second error correction decoder for error-correction decoding encoded data;

an interleaver memory for storing soft output decoded results calculated by a plurality of said first decoders as an interleaver input sequence; and

an interleave address generator for generating write addresses for storing said interleaver input sequence in said interleaver memory, and read addresses for randomly reading an interleaver input sequence stored in said interleaver memory,

wherein said interleave address generator adds an offset to a symbol number for said interleaver input sequence for correction, and converts the corrected symbol number for said interleaver input sequence to generate the read address when an address

for randomly reading the interleaver input sequence stored in said interleaver memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the interleaver input sequence.

7. A radio base station according to claim 6, wherein:

said interleave address generator specifies the symbol numbers for the interleaver input sequence as addresses at which the interleaver input sequence is stored in said interleaver memory, and

sequentially converts the symbol numbers for the interleaver input sequence stored in said interleaver memory to generate the read addresses for the interleaver input sequence stored in said interleaver memory.

8. A radio base station according to claim 7, wherein said interleave address generator comprises:

an output symbol number generator for sequentially generating symbol numbers for an interleaver input sequence stored in said interleaver memory; and

a threshold selector for setting a unique threshold for each of the symbol numbers generated by said output symbol number generator.

9. A radio base station according to claim 8, wherein:

said threshold selector selects a plurality

of thresholds in accordance with the number of information bits of said interleaver input sequence, wherein said thresholds each correspond to an output symbol number generated by said output symbol number generator for each of the number of information bits of said interleaver input sequence, said output symbol number generator possibly generating an address, the value of which exceeds the number of bits excluding tail bits from the number of information bits of said interleaver input sequence.

10. A radio base station according to claim 9, wherein:

said interleave address generator comprises an offset selector for selecting an offset, said offset being added to the output symbol number from said output symbol number generator, in accordance with a threshold value selected from said threshold selector.

11. A turbo encoder comprising:

a convolutional encoder for convolutional encoding transmission data;

an interleaver memory for storing transmission data; and

interleave address generator for generating write addresses for storing transmission data in said interleaver memory, and read addresses for randomly reading data comprising transmission data stored in said interleaver memory,

wherein said interleave address generator

adds an offset to a symbol number for each bit of the transmission data, and converts said corrected symbol number to generate the read address, when an address for randomly reading the transmission data stored in said interleaver memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the transmission data.

12. A turbo encoder comprising:

a plurality of convolutional encoders each for convolutional encoding information bits to be transmitted;

an interleaver memory for storing information bits to be transmitted; and

an interleave address generator for generating interleave addresses for randomly reading information bits stored in said interleaver memory,

wherein said interleave address generator converts a symbol number corresponding to an input symbol sequence to an address in accordance with a unique address conversion method to generate an interleave address, and corrects the symbol number in accordance with a previously determined rule and converts the corrected symbol number to generate the interleave address when the address converted from the symbol number does not match a previously set symbol number.

13. A turbo encoder according to claim 12, wherein:

said interleave address generator comprises logic circuits.

14. A turbo encoder according to claim 13, wherein said interleave address generator comprises:

an output symbol number generator for sequentially generating symbol numbers for an interleaver input sequence stored in said interleaver memory; and

a threshold selector for setting a unique threshold for each of the symbol numbers generated by said output symbol number generator.

15. A turbo encoder according to claim 14, wherein:

said threshold selector selects a plurality of thresholds in accordance with the number of information bits of said interleaver input sequence, wherein said thresholds each correspond to an output symbol number generated by said output symbol number generator for each of the number of information bits of said interleaver input sequence, said output symbol number generator possibly generating an address, the value of which exceeds the number of bits excluding tail bits from the number of information bits of said interleaver input sequence.

16. A turbo encoder according to claim 15, wherein:

said interleave address generator comprises an offset selector for selecting an offset, said offset

being added to the output symbol number from said output symbol number generator, in accordance with a threshold value selected from said threshold selector.